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Hybrid and Modular Multilevel Converter Designs for Isolated HVDC-DC Converters

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***Abstract*— Efficient medium and high voltage dc-dc conversion is critical for future dc grids. This paper proposes a hybrid multilevel dc/ac converter structure for use as the kernel of dc-dc conversion systems. Operation of the proposed dc/ac converter is suited to trapezoidal ac voltage waveforms. Quantitative and qualitative analyses show said trapezoidal operation reduces converter footprint, active and passive components size, and on-state losses relative to conventional modular multilevel converters. The proposed converter is scalable to high voltages with controllable ac voltage slope; implying tolerable *dv/dt* stresses on the converter transformer. Structural variations of the proposed converter with enhanced modularity and improved efficiency will be presented and discussed with regards to application in front-to-front isolated dc-dc conversion stages, and in light of said trapezoidal operation. Numerical results provide deeper insight of the presented converter designs with emphasis on system design aspects. Results obtained from a proof of concept 1-kW experimental test rig confirm the validity of simulation results, theoretical analyses, and simplified design equations presented in this paper.**

***Index Terms*— Modular multilevel converter, dc transformer, dual active bridge, dc fault, dc/dc power conversion**

I. Introduction

The economic challenges of bulk power transfer over long distances along with interface requirements of renewable generation have brought dc grids to the core of future energy plans. The evolution of dc grids, particularly at transmission levels, is impeded to date by the lack of efficient protection and loss management systems. Many point-to-point high voltage dc (HVDC) links are in operation or under construction at different dc voltage levels. Regardless of grid-wide loss management, dc-dc conversion provides a viable way to retrofit existing links as part of anticipated dc grids. In the absence of economic dc protection solutions, the active power electronics structure of potential dc-dc converters may be utilized to combine voltage matching and dc protection functions in one apparatus. Such a multi-functional apparatus needs to achieve the best compromise between cost, efficiency and power density.

With that in mind, many dc-dc conversion systems for medium/high voltage and high power have been proposed and analyzed in the literature. To ensure galvanic isolation, a dc-dc converter station design typically comprises two dc/ac converters connected through an ac transformer [1]. This is often termed front-to-front (F2F) connection, or dual active bridge (DAB) structure. Galvanic isolation may be needed in interconnections featuring dc lines of different ground arrangements or technology. On the other hand, compromising galvanic isolation introduces extra degrees of freedom in the dc-dc converter design process. Conceptually, non-isolated topologies may achieve higher power density due to the lack of bulky ac transformers. Some non-isolated dc-dc converter topologies may also feature higher efficiency should they use less power electronics switches in the conduction path. But known non-isolated dc-dc converter designs cannot offer as simple dc fault blocking capability – particularly for dc pole-to-ground faults – as F2F dc-dc converter topologies can. In the latter, dc fault blocking for pole-to-pole and pole-to-ground dc faults is simply realized by inhibiting solid-state switches of the healthy converter side [1, 2]. Yet, F2F dc-dc converters are likely to remain limited to onshore installations where galvanic isolation is mandatory.

A range of isolated and non-isolated F2F configurations has been shown to provide partial or full soft switching using either resonant stages [3-8] or modulation techniques [9-12]. The standard DAB or F2F structure employs two-level bridges producing phase shifted medium or high frequency square ac voltage waveforms to establish power flow through the ac link [12]. While suitable for low voltages, scaling to medium and high voltages applies intolerable *dv/dt* stresses upon ac link insulation (e.g. coupling transformer). Furthermore, series-connected semiconductor device strings (typically IGBTs) suffer voltage sharing problems and require complex gating and snubber circuitry [13].

Different resonant stages are often proposed to overcome the *dv/dt* problem and achieve wider soft switching ranges. Yet, in addition to their value drift problem, resonant tanks may experience high internal voltage stresses.

To overcome these obstacles, utilizing the standard modular multilevel converter (MMC) or the alternate arm converter (AAC) to build a medium frequency F2F connection was addressed in [14, 15]. Sinusoidal operation (i.e. sinusoidal ac waveform excitation of the ac link) facilitates the ac transformer design task. While it resolves many of the two-level DAB problems at high voltages, it requires significantly higher silicon area in addition to distributed energy storage elements (cell capacitors and arm inductors) contributing to a larger station footprint. Furthermore, soft-switching is compromised.

In [16] and [17], trapezoidal operation of conventional MMCs (i.e. production of trapezoidal voltage waveforms at the ac poles) was introduced and analyzed for use in DAB

converters so as to circumvent the shortcomings of square wave operation and relief the footprint penalty arising from the use of MMCs with sinusoidal ac voltages. Due to resulting structural variations, said design was denoted the 'quasi two-level converter' (Q2LC) in [16] and [17]. It offers a better utilization of the available dc voltage and merits relatively lower switching and on-state losses, and requires less installed semiconductor power than MMC counterparts. Furthermore, cells energy storage and arm inductances diminish, allowing footprint reduction. Although further investigation is required, ac transformer design could be facilitated by operating with so called six-step trapezoidal waveforms, in which three phase ac trapezoidal voltage waveforms with four dominant levels are produced, as presented in [17].

Several multi-module DAB structures have been introduced in an attempt to simplify ac transformer design via modularity. In such systems, dc-side power is split between several ac links [19, 20]. Series, parallel, or series-parallel connections lend the multi-module DAB design extra flexibility. An alternative approach utilizing F2F full scale MMCs has been proposed in [21, 22] where the voltage stepping is realized by the MMC cells, forming what can be termed an 'electronic dc tap changer'. On the down side, when the voltage gain of the lower-voltage-side MMC is higher than unity, each cell must be rated at the lower-voltage dc-link voltage. It is therefore best suited for medium and low voltage applications.

Along with isolated topologies, several non-isolated configurations have been proposed in pursuit of more compact dc-dc converter stations [23-27]. The so-called dc autotransformer was presented in [27] utilizing typical dc/ac MMC bridges in analogy to the ac autotransformer. Also, a 'modular multilevel dc converter' was presented in [28]. Two versions were derived, namely the tuned-filter and the push-pull converters. While the former requires large passive filter components, the latter was analyzed in detail in [19] for different design scenarios and shown to incur more cost in comparison to an equivalent multi-module DAB. The single stage topology in [25], termed DC-MMC, is another variation of the stated modular multilevel dc converter of [28]. While the installed converter power in the DC-MMC may be less than equivalent F2F configurations, the presented analysis shows that large coupled inductors may need to be fitted in the output side.

To address some of the highlighted challenges, this paper presents in depth analysis of a dc/ac converter structure denoted 'the transition arm converter' (TAC). It further compares it to the Q2LC and the so-called controlled transition bridge (CTB), with emphasis on utilization in dc-dc converters. The CTB concept was originally proposed in [30] for HVDC voltage source converter (VSC) stations operating with trapezoidal ac waveforms, but not analyzed for use in dc-dc converters. The contribution of this paper can be summarized as follows:

- In depth design aspects of TAC structure are presented. Specifically, evaluation of the semiconductor power, energy storage requirements, and incurred steady state losses are given in comparison to the Q2LB and the CTB structures with regards to trapezoidal modulation.
- Modular TAC structures are proposed and analysed for use in high voltage F2F dc-dc converters. In addition to full converter modularity, these modular TAC structures will be shown to offer further merits in terms of efficiency with respect to dc-dc conversion applications.
- Experimental validation of the TAC concept is provided using a scaled 1kW test rig.

The paper is organized as follows: section II briefly introduces the basic TAC structure highlighting its merits with respect to the Q2LC and the CTB for operation with trapezoidal ac waveforms. Section III presents a detailed high-power simulation scenario for a TAC-based F2F dc-dc converter in comparison to the CTB case. Section IV details TAC design in terms of semiconductor device ratings, energy storage, and losses, highlighting its merits over the CTB and Q2LC by comparative analysis. Section V proposes and validates modified fully-modular TAC designs for use in high power dc-dc converters. Section VI presents proof-of-concept experimental results for the basic TAC converter bridge. Finally, conclusions are drawn and discussed.

II. TAC Structure for Trapezoidal AC voltages

A. The Basic Transition Arm Converter

The basic TAC is a hybrid dc/ac bridge structure in which each phase leg comprises a *bi-state* arm and a *transition arm* (refer to Fig. 1a). The bi-state arm resembles a two-state switch valve which can be realized as a series semiconductor switch array. The transition arm is composed of series connected half bridge (HB) cells in a similar structure to a traditional MMC arm (Fig 1a). Each HB cell in the transition arm comprises a *power* path in which a high-power switch is connected and an *auxiliary* path (circuit) in which an auxiliary low-power switch is connected in series to cell capacitor. In TAC, the auxiliary circuit in each HB cell operates mainly as an active voltage clamp. The number of HB cells per transition arm must be sufficient to block the full dc voltage as in a conventional MMC arm.

Each phase leg of TAC in Fig. 1a uses transition arm HB cells to synthesize ac voltage waveforms at the ac poles 'a', 'b' and 'c', with discrete voltage steps dictated by individual HB cell capacitor voltages. States '0' and '1' are defined for each HB cell. State '0' stands for the switching state in which the cell capacitor is bypassed by turning on the power switch. State '1' represents the switching state in which the cell capacitor is inserted into the power path by activation of the auxiliary switch while power switch is in off state. A further switching state '2' in which both power and auxiliary switches are turned off, is also defined for each HB cell and is denoted 'idle' state henceforth.

The switching sequence in TAC is controlled, as exemplified in Fig. 2, such that each bi-state arm is turned on or off only when all HB cells of the respective transition arm are in state '1'; otherwise, it must remain at off state. Operation of TAC in this manner allows controlled gradual voltage transition across each bi-state arm. Consequently, the on or off switching of each bi-state arm can be administered when the voltage across its terminals is zero or near zero, leading to trivial switching losses in bi-state arms.

Synthesis of a staircase approximated trapezoidal voltage waveform offers a good utilization of the TAC structure. For a trapezoidal ac output voltage waveform having a positive

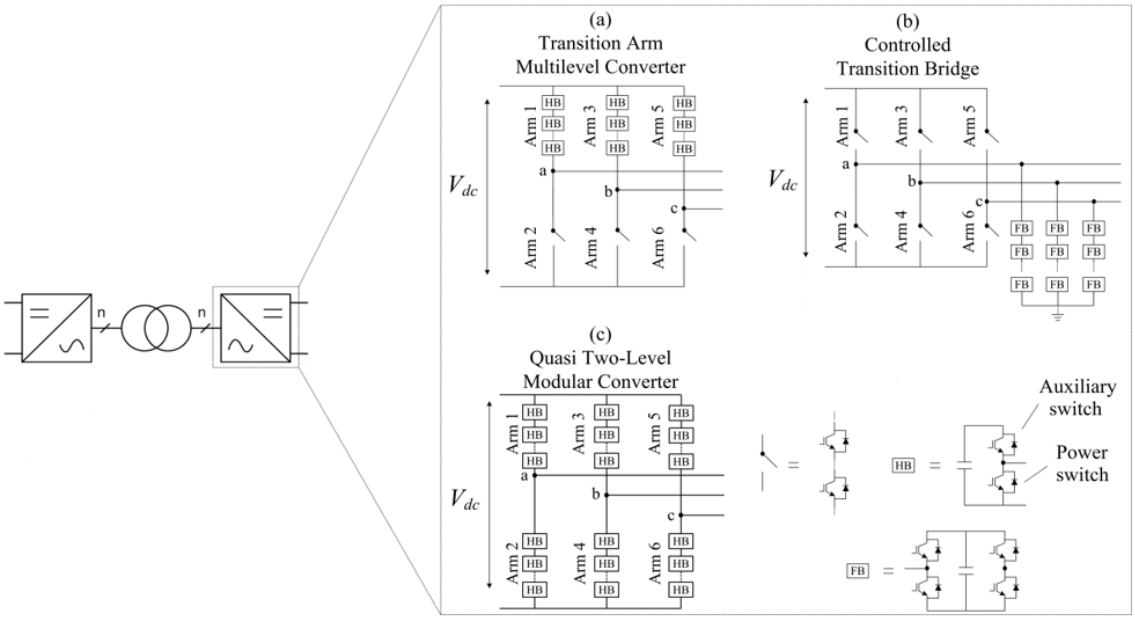


Fig 1. Bridge structures suitable for DAB with trapezoidal waveforms.

dominant level and a negative dominant level. With reference to Fig. 1a and Fig. 2, said positive dominant ac voltage level (+½V_{dc}) is produced when transition arm cells in the respective phase leg are all in state '0' and the respective bi-state arm is off. When the bi-state arm is off, full ac pole current flows in the transition arm. Said negative dominant ac voltage level (–½V_{dc}) is produced at said ac pole when all said transition arm cells are in state '1' and said bi-state arm is on and full ac pole current flows therethrough. At ac pole voltage transition from –½V_{dc} to +½V_{dc}, the bi-state arm turns off, then transition arm cells switch sequentially from state '1' to state '0' with a time step (dwell time) T_d in a total voltage transition interval T_t. Likewise, ac pole voltage transition from +½V_{dc} to –½V_{dc} is realized by sequential switching of transition arm cells from state '0' to state'1' with a dwell time T_d, then the bi-state arm turns on.

When TAC operates with relatively high gradient trapezoidal ac waveforms, HB cells of each transition arm serve as energy tanks only during the controlled voltage transition interval T_t between the two dc rail voltage levels, which can be made as short as a couple of tens of microseconds. This implies a reduced energy storage requirement for transition arm HB cell capacitors and, consequently, a reduced footprint.

B. TAC versus CTB and the Q2LC

The Q2LC, the CTB are two other dc/ac bridge structures suitable for operation with trapezoidal ac waveforms. The Q2LC discussed in [16] and [17] is basically an MMC operated as a two-level converter generating relatively high gradient trapezoidal ac voltage waveforms at the fundamental frequency. It resembles typical MMC structure with reduced volume of cell capacitors and semiconductor ratings. The fact that TAC replaces one cascaded HB arm in each phase leg of the Q2LC with a director switch implies lower semiconductor

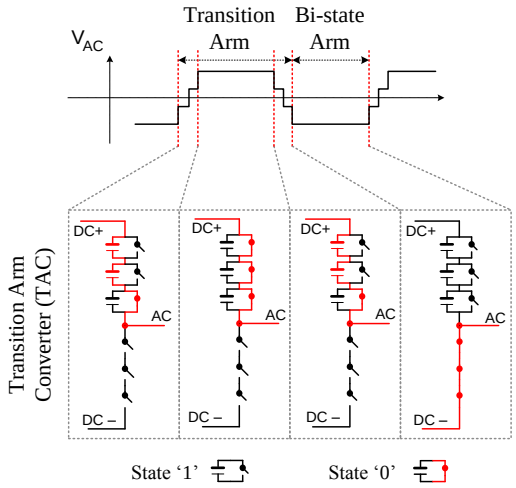


Fig.2 Switching sequence of an illustrative 4-level TAC phase leg synthesizing a trapezoidal ac voltage waveform [red traces carry load current].

ratings and less energy storage with respect to the Q2LC, as will be shown in section IV.

On the other hand, the CTB (shown in Fig. 1b) comprises bi-state switches (director switches) in the main power stage, forming a six-pulse bridge, as well as three limbs of cascaded full-bridge (FB) cells (chain-links) connected between dc ground and ac poles 'a', 'b' and 'c' [30]. The FB cells of each limb are used to facilitate discrete stepped transition between positive and negative dc rails and this is realized by sequential insertion of the FB cell capacitors to synthesize trapezoidal ac waveforms at ac poles 'a', 'b' and 'c'. The cascaded FB cells in each chain-link of the CTB converter need to be able to block only half the dc link voltage (½V_{dc}). Furthermore, director switches in a CTB turn on and off at nearly zero voltage as in

TAC; therefore, low switching losses are achieved in the six-pulse bridge of a CTB [29].

A salient advantage of TAC and CTB over the Q2LC is that the voltage across bi-state arms and director switches during switching is controlled by the chain-links and, consequently, series arrays of thyristors can be employed therein which boosts converter efficiency. Chain-links are used to provide sufficient reverse voltage across thyristors to turn bi-state arms of TAC and director switches of the CTB off [30]. On the other hand, a salient demerit of the CTB is that in practice the converter station valve hall will accommodate two separate bridge structures; a six-pulse bridge and the cascaded FB chain-links. This poses a design and cost burden. As opposed to that, TAC or Q2LC would be practically built such that the valve hall accommodates a single bridge which. The Q2LC valve hall is expected to resemble a typical MMC valve hall layout albeit with a reduced footprint. While the Q2LC is a fully modular converter design, TAC is a hybrid structure; however, the basic TAC structure can be reconfigured to achieve a full modular TAC design as will be detailed in section V.

The discussion and analysis in the following sections will only consider the use of force commutated devices in the bi-state arms and the director switches for space limits. Operation and control of TAC and the CTB for operation with thyristors will be left to future work.

III. Full-Scale Isolated DC-DC Structure

Although the dc/ac converter structures addressed in section II can be utilized as the kernel of either isolated F2F dc-dc converters or so-called dc autotransformer designs, this paper considers the F2F dc-dc converter topology only due to space limits. Expansion of the analysis and design methodology carried out in this paper to the dc autotransformer case is quite straightforward and can be left to the reader or treated in future research. However, it is worth noting that, regardless of dc/ac bridge structure, non-isolated dc-dc converter designs require conceptually more complex mechanisms of dc fault blocking (particularly pole-to-ground faults) in comparison to isolated F2F dc-dc converter designs which offer natural dc fault blocking as highlighted in [16]. This should also be taken in consideration on selection of the suitable dc-dc converter design for a certain HVdc connection.

In the standard F2F dc-dc converter, a single three-phase ac transformer, or three single-phase ac transformers, couples two dc/ac converters each rated at the full converter power. Power flow magnitude and direction are controlled by the vectorial relationship between respective ac pole voltages of the two dc/ac converters and the leakage reactance (L_s) of the coupling transformer. The ac link of the considered F2F dc-dc converter configurations is excited at frequencies higher than ac power frequency but bounded to a few hundred hertz to tradeoff power density and losses [17]. As pointed out in [19], tenfold increase of power density relative to 50 Hz designs is observed at 1kHz fundamental frequency in the ac link.

Producing a trapezoidal ac voltage waveform of many intermediate voltage levels at such frequency range and at high voltage limits the maximum attainable fundamental voltage as well as controllability, as detailed in [17]. When no medium voltage cells are employed (e.g. as used in ABB's cascade two-level converter [31]), cells of TAC, CTB, or the Q2LC may be grouped in subgroups each producing a sizable intermediate voltage step, subject to *dv/dt* tolerances. This reduces the number of levels in the ac pole voltage waveform from N+1 to N_s+1 where $N_s = \lceil N / n \rceil$, N being the number of cells per arm and n being the number of cells in each subgroup [17]. Cells within each subgroup have the same switching state and are switched simultaneously, as demonstrated in [17] for the Q2LC case.

In a dc grid application at steady-state, F2F dc-dc converters feature limited dc ratio (ρ) variations, where $\rho = b/a$; b being the ratio between primary side and secondary side dc voltages and a being the coupling transformer turns ratio (Fig. 3b). Consequently, modulation index control and load power factor (load angle) ranges for a F2F dc-dc converter ac link will be tighter than for a dc/ac conversion station due to the limited variations in dc voltages at different loading conditions. In such a case, trapezoidal operation is best utilized. Modulation index of each dc/ac converter can be varied for steady state conditions by manipulating trapezoid slopes within a certain range in conjunction with auxiliary methods, if required, as discussed in [17].

In comparing different aspects of the three converters of Fig. 1, a simulation scenario is set up in Matlab/Simulink® where each converter type is employed as the kernel of the 60 MW F2F full scale dc-dc converter of Fig. 3b. Said F2F dc-dc converter is fed from two stiff dc sources each connected to one dc side of the considered F2F dc-dc converter through a small series impedance to simulate some level of dc voltage ripple. Each primary and secondary three phase converter is modeled such that each ac pole produces 11-level (N_s+1) trapezoidal voltage waveform with reference to respective virtual ground point (which is a virtual dc link midpoint). The ac link coupling transformer is not grounded; hence, the voltage of each ac pole with reference to respective ac transformer neutral point is a multilevel trapezoidal waveform with four dominant levels at $\pm\frac{1}{3}V_{dc}$ and $\pm\frac{2}{3}V_{dc}$ and intermediary voltage levels [17]. This type of waveform is denoted 'six-step trapezoid' henceforth. Fig. 3a show six-step trapezoidal ac voltage waveforms of a primary side ac pole v_p and of the corresponding secondary side ac pole referred to primary side v_s, as well as the related ac pole currents referred to primary side. In Fig. 3a, φ refers to the phase shift angle between respective primary and secondary ac pole voltages, ω_s is the angular fundamental frequency (which is also the switching frequency), and subscripts p and s refer to primary and secondary side parameters. Common simulation parameters are given in Table I.

The considered simulation scenario of the same parameters shown in Table I has been conducted in [17] for a Q2LC-based F2F dc-dc converter and the reader may refer to [17] for comparison.

When TAC is used as the kernel of the F2F dc-dc converter of the current simulation scenario, each transition arm is modeled as a series connection of thirty 3.3kV HB cells for operation with $N_s = 10$ (i.e. each subgroup employs three cells; $n = 3$). Each cell employs Infineon's IHV FZ1500R33HL3 IGBT (1500A) for the power path and FZ400R33KL2C (400A) for the auxiliary path. This number of cells per transition arm provides a level of redundancy at 2kV per cell.

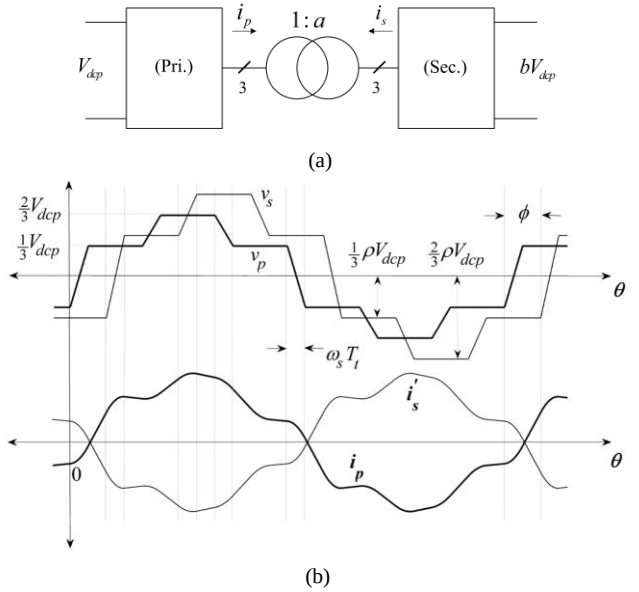


Fig.3 The generic full scale front-to-front dc-dc converter structure (a) ac link waveforms, and (b) single line diagram.

TABLE I
PARAMETERS OF THE SIMULATED THREE-PHASE DC-DC CONVERTER

	Primary side	Secondary side
DC voltage (V_{dc})	±30kV	±60.6kV
DC side inductance (L_{dc})	1mH	1mH
DC side resistance (R_{dc})	0.1Ω	0.1Ω
DC ratio (ρ)	1.01	
Load angle (φ)	7.2°	
Active power flow	60 MW	
Dwell time (T_d)	5μs	
DC link capacitor (C_{dc})	25μF	
Operating frequency (f_s)	250 Hz	
Coupling transformer	55 kV/110 kV - power: 63MVA series inductance: 10% - series resistance: 0.3% - Base impedance: 48.2Ω at the 55kV side	

Respective datasheet on-state characteristics are considered in the model and 0.5μH stray inductance is modeled per cell. Each bi-state arm employs thirty series-connected IHV FZ1500R33HL3 3.3kV/1500A IGBTs. For faster simulation, the secondary side is modeled using ideal switches with $N = N_s = 10$ and the same dwell time as the primary side.

Main observations of the above simulation scenario are summarized in Fig. 4a which shows waveforms depicted from the primary side TAC. It can be observed that cell voltages exhibit about ±12% ripple in the viewed transition arm for the modeled cell subgroup capacitance of 8μF. The bounded voltage ripple is achieved using the traditional sorting algorithm with the transition arm current and cell voltages sampled four times per fundamental cycle – and not during voltage transition intervals – and cells are sorted for sequential switching in ascending or descending order subject to transition arm current direction.

The arm currents in the viewed TAC phase leg can be seen to flow in one phase arm at a time except for the voltage transition intervals. Power path IGBTs of HB cells take up the whole load current for most of the fundamental cycle while auxiliary IGBTs carry discontinuous current pulses only for an interval T_t during ac pole voltage transitions; that is, when cell capacitors are involved in power transfer (Fig. 4a). As soon as the bi-state arm switches on, insignificant common mode balancing current is interchanged with the dc side to balance the phase leg voltage. As observed, no dedicated arm inductance is required where the modeled 5μH per cell stray inductance proved sufficient.

Calculation of ac link currents has been carried out in [17] for a Q2LC-based F2F dc-dc converter. The developed mathematical forms are valid for a generic F2F dc-dc converter utilizing Q2LC, TAC, or a CTB. Based on that, the peak value of ac pole (arm) current of the primary side converter i_p^{pk} can be calculated as in (1). The interested reader may revise [17] for derivation f (1).

$$i_p^{pk} = \frac{V_{dcp}}{3\omega_s L_s}\left((\rho - 3 + \frac{2}{\rho})\omega_s T_t + 2\varphi + (\rho - 1)\frac{\pi}{3}\right) \quad (1a)$$

$$T_t = (N_s - 1)T_d \quad (1b)$$

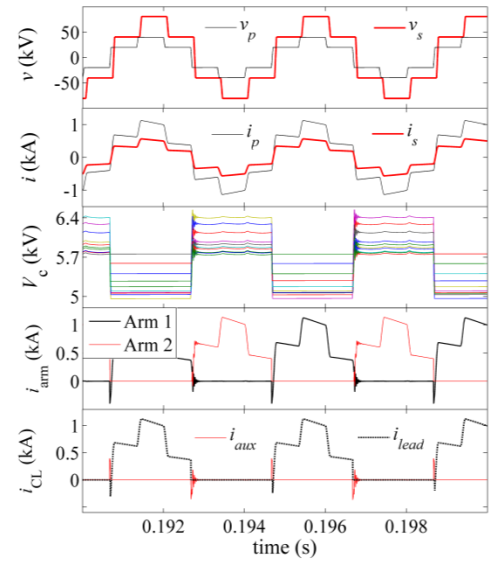
Where V_{dcp} is the primary dc side voltage. Considering the parameters of Table I, (1) results in a peak ac pole current of about 1080A at the primary side TAC. Fig. 4a shows that the numerically simulated value of primary side peak ac pole current is about 1130A, which is in good agreement with the value calculated by (1) given the assumptions made in its derivation (e.g. negligence of ac link resistance).

When CTB is used as the kernel of the F2F dc-dc converter of the current simulation scenario with $N_s = 10$, the same 3.3kV 400A IGBT modeled for auxiliary circuits of TAC cells is employed for the primary side CTB chain-link FB cells. In this case, each chain-link will need to employ 20 FB cells to realize the transit between the two dc rails (±30kV) with 1.5 kV per cell and $n = 2$. Each director switch is modeled as a series connection of the IHV FZ1500R33HL3 3.3kV/1500A IGBT modules.

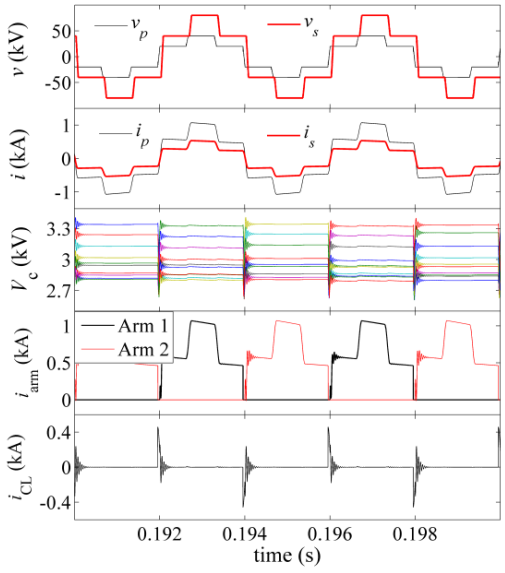
As evident in Fig. 4b, the six-pulse bridge supplies full load current, whereas the chain-links exchange energy with the load only during the brief voltage transitions between positive and negative dc rails, featuring short-duration low current particularly at low load angles. The peak current in each chain link occurs when its corresponding upper or lower director switch is turned on. The sample plot for chain link current in Fig. 4b confirms that the FB cells in each chain-link of CTB converters can use switching devices with significantly lower continuous current rating relative to these of director switches. According to Fig. 4b, the director switch currents in each phase leg are alternate and show good agreement with the primary side peak ac pole current given in (1). Cell voltages in a sample chain-link are depicted where a voltage ripple of about ±13% is achieved with 32μF modeled cell capacitance and using the traditional sorting algorithm for voltage balancing.

IV. TAC MERITS W.R.T CTB AND Q2LC

This section investigates the relative advantages TAC structure offers with respect to the CTB and the Q2LC under trapezoidal operation through quantitative analyses of optimum cell capacitance, current ratings, and losses in each bridge structure.



(a)



(b)

Fig.4 Primary side numerical simulation results of the front-to-front converter when it is (a) TAC-based and (b) CTB-based.

A. *Net Energy Exchange*

To ensure proper operation of any of the converters of Fig. 1, and hence a controlled voltage traverse between the dc rails, cell voltages must not drift away from their set-points. An essential requirement is a near zero net energy exchange (gain) by each phase leg/chain-link over a fundamental cycle. If this requirement is satisfied, the conventional sorting algorithm will be sufficient to produce near equal voltage steps [14].

The net energy exchange of an arm over a fundamental cycle depends on converter structure, switching sequence, and loading. This is investigated for the three converters of Fig. 1 when each is used as the kernel of a three-phase F2F converter with a load angle range $\omega_s T_t \geq \varphi \geq \frac{1}{3}\pi$. The net energy exchange ΔE_{arm} of an arm within one voltage transition interval T_t in any of the converters of Fig. 1 can be generically calculated as in (2a).

$$\Delta E_{arm} = \frac{1}{\omega_s}\int_{\theta_o}^{\theta_o+\omega_s T_t} V_{arm}(\theta) i_{arm}(\theta) d\theta \tag{2a}$$

where $V_{arm}(\theta)$ and $i_{arm}(\theta)$ are the voltage difference across the arm and the current through the arm. Starting with TAC, the net energy exchange of a transition arm due to ac pole current flow in HB cells capacitors over a fundamental cycle is;

$$\Delta E_{TA} = \Delta E_1 + \Delta E_2 \tag{2b}$$

where subscript *TA* refers to transition arm. ΔE_1 and ΔE_2 are the energy gains during both voltage transition intervals in a fundamental cycle. Assuming the considered TAC is utilized in the primary side of said F2F dc-dc converter, and $\theta = 0°$ at the instant the bi-state arm of the same phase leg switches off, then;

$$\Delta E_1 = \frac{1}{\omega_s}\int_0^{\omega_s T_t}\left[\frac{1}{2}V_{dcp} - v_p(\theta)\right] i_p(\theta) d\theta \tag{2c}$$

$$\Delta E_2 = \frac{1}{\omega_s}\int_{\pi}^{\pi+\omega_s T_t}\left[\frac{1}{2}V_{dcp} - v_p(\theta-\pi)\right] i_p(\theta-\pi) d\theta \tag{2d}$$

$i_p(\theta)$ and $v_p(\theta)$ are the ac pole current and voltage at the primary side, respectively. Full calculation of primary ac pole current in a generic F2F converter topology is irrelevant to dc/ac converters internal structure and is possible given the absence of dc offset in phase currents [9, 17]. For trapezoidal operation, with $\theta_o = 0$ and $\omega_s T_t \geq \varphi \geq \frac{1}{3}\pi$, primary side ac pole-to-ground voltage and ac pole current for the voltage transition interval corresponding to $0 \leq \theta \leq \omega_s T_t$ are;

$$v_p(\theta) = V_{dcp}\left(\frac{\theta}{\omega_s T_t} - \frac{1}{2}\right) \tag{3a}$$

$$i_p(\theta) = \frac{V_{dcp}}{3\omega_s L_s}\left(\frac{1}{\omega_s T_t}\theta^2 + (\rho-1)(\theta + \frac{2}{3}\pi - \frac{1}{2}\omega_s T_t) - \rho\varphi\right) \tag{3b}$$

The reference current direction is out of the primary side ac pole. For a balanced F2F connection in steady state, $i_p(\theta) = -i_p(\theta \pm \pi)$ and $v_p(\theta) = -v_p(\theta \pm \pi)$. Using this half-symmetry property, (2) can be simplified such that the net transition arm energy exchange ΔE_{TA} can be quantified as in (4a).

$$\Delta E_{TA} = -\frac{2}{\omega_s}\int_0^{\omega_s T_t} v_p(\theta) i_p(\theta) d\theta \tag{4a}$$

Substituting (3) in (4a);

$$\Delta E_{TA} = -\frac{V_{dcp}^2 \rho T_t^2}{18 L_s} \tag{4b}$$

Equation (4b) confirms a non-zero transition arm net energy exchange by ac pole current flow through HB cell capacitors over a full cycle. Over the indicated load angle (φ) range (i.e. $\omega_s T_t \geq \varphi \geq \frac{1}{3}\pi$), where the TAC is inductively loaded [17], (4) shows that ΔE_{TA} is negative, implying transition arm energy storage is curtailed. Equation (4) further demonstrates that the amount of energy curtailment is decoupled from the load angle φ. This can be concluded with a careful inspection of TAC switching sequence and ac pole voltage and current waveforms during ac pole voltage transition. The non-zero value of ΔE_{TA} means that the aggregate voltage of transition arm cells becomes lower than the dc link voltage at $\theta = \pi + \omega_s T_t$, which is the instant the bi-state arm switches on. This voltage

imbalance will trigger a common mode current. The latter acts to charge the transition arm to the dc link voltage; thus, bringing the net transition arm energy exchange over the cycle to zero.

In the case when the primary side converter is a CTB with same operating conditions, the dynamics governing the net energy exchange of chain-links are different from a TAC case. Herein, the net energy exchange of each chain-link rounds to zero each half a fundamental cycle. Calculation of the net energy exchange must consider the bipolar voltage output of each chain-link. For that, the chain-link charging direction is always taken the reference current direction. Note the reference direction reverses with chain-link voltage polarity reversal. Under inductive loading, and assuming $\theta = 0°$ at the instant ac pole voltage starts transition towards the positive dc rail, chain-link energy gain during the considered voltage transition interval ΔE_{ch} will be;

$$\Delta E_{ch} = -\frac{1}{\omega_s}\int_0^{\omega_s T_t} v_p(\theta) i_p(\theta) d\theta = -\frac{V_{dcp}^2 \rho T_t^2}{36 L_s} = -\frac{V_{dcp} V_{dcs} T_t^2}{36 a L_s} \qquad (5)$$

$i_p(\theta)$ and $v_p(\theta)$ are given in (3). Equation (5) shows that the chain-link energy gain is negative. This implies energy is exported from the chain-link to the load side (ac link transformer). The exported amount of energy will be instantly restored back from the dc side when the complementary director switch ties the respective ac pole to the positive dc rail. A similar mechanism takes place during the second voltage transition interval in the cycle. Similar to transition arms of TAC, (5) indicates that chain-links energy exchange is decoupled from the load angle φ. This is predictable since bipolar cell capacitors reverse polarity during T_t whereas chain-link current does not exhibit polarity reversal (for the said operating region).

In the case when the primary side converter is a Q2LC with same operating conditions, assuming said Q2LC operates with the non-complementary switching (NCS) sequence detailed in [17], each arm exchanges a net amount ΔE_{arm} of energy once per fundamental cycle. With careful inspection of current flows within a Q2LC under said switching sequence as presented in [17], it is observed that the energy exchange in both arms of a phase leg due to load current flow through respective cell capacitors over a fundamental cycle is of the same polarity (positive or negative, subject to loading conditions). It can be shown that in steady state inductive loading, the energy gain in each arm ΔE_{arm} is as given in (6).

$$\Delta E_{arm} = \frac{V_{dcp}^2 T_t}{36 \omega_s L_s}\left[6\rho\varphi - 4\pi(\rho - 1) - (\rho + 2)\omega_s T_t\right] \qquad (6)$$

Despite the non-zero energy gain during ac voltage transit shown in (6), the net energy exchange per cycle in each arm is kept near zero by action of the common mode current triggered when the ac pole gets tied to the opposite dc rail.

The conclusion is that the energy-storing-arms in each of the three considered converter types feature near zero net energy exchange per fundamental cycle in steady state under inductive loading. This holds also for capacitive loading and can be proven in a similar manner. Consequently, cell rotation using conventional sorting algorithms normally used for MMC is enough to retain cell voltages within a desired ripple band in steady state. This is shown in Fig. 4 for the TAC and CTB, and is experimentally confirmed for the Q2LC in [17] and for TAC in section VI.

B. Cell Capacitance Design

An informative comparison between the three converters of Fig. 1 requires knowledge of installed arm/chain-link energy storage. Cell capacitors regularly rotate to the top rank of the sorting algorithm; hence each capacitor in the arm/chain-link must be sized to endure current flow for an interval T_t. Design of cell subgroup capacitance can be performed by knowledge of arm/chain-link current during T_t, as well as the maximum and minimum values of ρ; as has been shown in [17] for the Q2LC. A simplified method is adopted herein, in which capacitance design is performed at $\rho = 1$ while introducing a compensating (safety) factor to account for ρ variation range. This way, cell subgroup capacitance C_{gp} of primary and secondary sides can be calculated from the basic definition of capacitance value for a maximum permissible voltage ripple band, as in (7).

$$C_{gp} = \gamma \frac{\lambda N_s}{\ell \omega_s V_{nom}} \int_{\pi}^{\pi + \omega_s T_t} i_p(\theta - \pi)\, d\theta \qquad (7a)$$

$$C_{gs} = \frac{1}{a^2} C_{gp} \qquad (7b)$$

Equation (7b) is valid when primary and secondary sides of a F2F dc-dc converter have equal transit times T_t. Using said symmetry property and (3), (7a) reduces to (7c).

$$C_{gp} = \gamma \frac{\lambda V_{dcp} N_s T_t}{3 \ell \omega_s L_s V_{nom}}\left(\varphi - \frac{1}{3}\omega_s T_t\right) \qquad (7c)$$

In (7), ℓ is the per unit subgroup capacitor voltage change, γ is a safety factor to account for the operational range of ρ and effect of arm/chain-link voltage balancing overshoot. V_{nom} is the nominal arm/chain-link voltage. $V_{nom} = V_{dcp}$ for the TAC and Q2LC cases, and $V_{nom} = ½V_{dcp}$ for the CTB case. Note that (7) is valid for $\omega_s T_t \le \varphi \le ⅓\pi$.

A constant λ is introduced in (7) to represent the ratio between required energy storage in the three converter types operating under same conditions. The constant λ equals ½ for the TAC and 1 for the Q2LC and the CTB. The reason for the introduction of such a ratio is that, unlike Q2LC and CTB, each TAC transition arm undergoes two energy excursions of opposite polarities per steady-state fundamental cycle before its voltage balances back with the dc link. Thus, cell capacitance in a TAC is nearly half that of an equivalent Q2LC in which each arm of a given phase leg undergoes a single energy excursion – given by (6) – due to load current flow therethrough. Said load current flow in each arm occurs during only one voltage transition interval per fundamental cycle (under NCS switching sequence).

For operating conditions of Table I, (7c) for ±10% cell voltage ripple ($\ell = 0.2$) and $\gamma = 1$ gives 8μF, 32μF, and 16μF for the TAC, CTB and the Q2LC, respectively. Numerical simulation according to Table I using these capacitance values shows that cell voltage ripple is ±13% to ±14%. The mismatch is due to approximations involved in developing (7), for instance, the negligence of ac link series resistance. To bring the cell voltage ripple figure down to near ±10%, the safety factor is found to be about 1.3 to 1.5 (depending on converter

type). If the conditions of Table I are considered rated conditions (i.e. $\varphi = \varphi_{max}$), then C_{gp} design values for near ±10% cell voltage ripple, using the updated safety factor values, are approximately 11µF, 44µF, and 23µF for TAC, CTB and the Q2LC, respectively. These values mean that the primary side cell capacitance, after accounting for n, is approximately C_{cell} = 30µF (TAC), C_{cell} = 70µF (Q2LC), and C_{cell} = 90µF (CTB). Secondary side cell capacitances can be accordingly calculated using (7b). Observe that cell capacitance values are significantly smaller than conventional MMCs, confirming considerable footprint gain. It is worth noting that the ±10% voltage ripple target is taken as an illustrative example and is not suggested as an optimum ripple value for the considered application.

C. Switching Devices Current Rating

Equation (1a) defines the peak phase current only for $\rho \geq 1$. Alternatively, the design process for power path semiconductor devices in each cell will be shown to be valid for the whole operating range of ρ values by designing for $\rho = 1$ and using a suitable safety factor. At $\rho = 1$, (1a) reduces to (8).

$$i_p^{pk} = \gamma_r \frac{2V_{dcp}\varphi}{3\omega_s L_s} \quad , \quad i_s^{pk} = \gamma_r \frac{2V_{dcp}\varphi}{3\rho a\omega_s L_s} \tag{8}$$

Where i_s^{pk} is the secondary side peak phase current. While the range of ρ is minimal for the considered dc grid applications, (8) at $\varphi = \varphi_{max}$ will provide an acceptable design estimate given the high level of rating redundancy (represented by γ_r) normally considered when selecting semiconductor devices ratings. Equations (1a) and (8) provide values in close agreement with simulated value of Fig. 4. Observe that selected switching devices current ratings in HB cells power paths, bi-state arms, and in director switches in that particular simulation set up considers a safety factor of $\gamma_r \approx 1.5$ according to (8).

Rating auxiliary circuit/chain-link switching devices can be similarly carried out by calculation of ac pole current during voltage transition intervals. From (3b) at $\theta = 0°$;

$$i_{px}^{pk} = \frac{V_{dcp}}{3\omega_s L_s}\left((\rho-1)\left(\frac{2}{3}\pi - \frac{1}{2}\omega_s T_t\right) - \rho\varphi\right) \tag{9a}$$

At $\rho = 1$, ignoring current polarity, design values for primary and secondary side auxiliary circuits/chain-links are given by (9b).

$$i_{px}^{pk} = \frac{V_{dcp}\varphi}{3\omega_s L_s} \quad , \quad i_{sx}^{pk} = \frac{V_{dcp}\varphi}{3\rho a\omega_s L_s} \tag{9b}$$

i_{px}^{pk} and i_{sx}^{pk} are the primary and secondary side auxiliary circuit/chain-link peak currents. It is observed that the current in (9b) is half the current of (8) when $\gamma_r = 1$, which is predictable. As seen in Fig. 4, the auxiliary circuit/chain-link currents are not continuous, rather of pulsating nature. Therefore, it will be considered of sufficient redundancy to rate switching devices to the peak pulse current of (9b) for $\varphi = \varphi_{max}$. Comparing (8) and (9) when $\gamma_r \approx 1.5$ for redundancy, one concludes that the current rating of auxiliary circuit/chain-link switching devices is around one-third that of HB cells power paths, bi-state arms, and director switches.

D. Semiconductor Effort and Storage Capacity

The installed apparent power in each converter type, denoted here *the semiconductor effort*, can now be calculated given device voltages and current ratings V_d and I_d, respectively. V_d is equal to nominal cell voltage (V_{dc}/N). V_d is equal to nominal cell voltage (V_{dc}/N). For instance, the semiconductor effort of one IGBT/diode pair module is V_dI_d. The purpose here is to provide a figure of merit with respect to the relative semiconductor area installed in each type of converter, rather than quantify the precise amount/number of power electronics components installed in each type of converter with consideration of reliability and redundancy.

Note that auxiliary/chain-link devices are rated here at $⅓I_d$ (section IV.*C*). Table II summarizes the semiconductor effort of each converter relative to the standard two level converter of same power rating. It is evident that the TAC offers lowest semiconductor effort after the standard two-level converter.

With reference to Table II, the semiconductor effort of the considered F2F dc-dc converter is found to be $14NV_dI_d$ when it is TAC-based, $16NV_dI_d$ when CTB-based (or Q2LC-based), and $15NV_dI_d$ when one side is a TAC and the other is a CTB (or a Q2LC). These values are independent of the ratio between dc voltages. These figures confirm an outstanding semiconductor effort advantage for the considered F2F dc-dc converter configurations with trapezoidal operation relative to the MMC-based F2F connection with sinusoidal operation. An approximation of the latter's semiconductor effort can amount to $12NV_dI_d$ per dc/ac converter (i.e. $24NV_dI_d$ in total) assuming half-bridge cells are employed. This approximated figure ignores circulating arm currents in each MMC and the ratio between fundamental components of trapezoidal and sinusoidal ac voltage waveforms when synthesized from the same dc-side voltage. One can conclude that an MMC-based F2F dc-dc converter is significantly more demanding, semiconductor-wise, than trapezoidal-operated F2F dc-dc converter counterparts, which promises a considerable reduction of power electronics cost.

The installed energy storage capacity in each converter can be quantified using (7). It can be observed from (7c) that TAC subgroup capacitance is half that of the Q2LC, which is in turn half that of the CTB. Simple calculations show that the total installed energy storage in the TAC and the CTB is equal to $1.5C_g(V_{dc})^2/N_s$ with C_g being the subgroup capacitance. This figure is one-fourth of the installed storage capacity in the Q2LC.

Consequently, one can conclude that semiconductor effort and installed storage capacity may give the TAC a capital cost advantage over the other counterparts for the considered dc grid application.

TABLE II
SEMICONDUCTOR EFFORT OF THE THREE TYPES OF CONVERTERS AND THE TWO-LEVEL COUNTERPART

Converter	Semiconductor effort	Modulation
Two-level	$6NV_dI_d$	Square
Q2LC	$6NV_dI_d + 6NV_d \times ⅓I_d = 8NV_dI_d$	Trapezoidal
CTB	$6NV_dI_d + 3\times½N\times4V_d\times⅓I_d = 8NV_dI_d$	Trapezoidal
TAC	$6NV_dI_d + 3\times N\times V_d\times⅓I_d = 7NV_dI_d$	Trapezoidal

E. Converter Losses

For $\varphi \geq \omega_s T_t$ both converters of a F2F connection are inductively loaded and, consequently, all HB and FB cell IGBTs will exhibit soft turn on and hard turn off, as detailed in [17]. This property holds for the three considered converter types. Turn-off switching losses can be significantly curtailed by lossless capacitive snubbers [19]. Hence, the converters will be considered offering negligible overall switching losses, given also the zero voltage switching property of bi-state arms and director switches.

The conduction power loss in a solid-state switching device is;

$$P_{loss} = \frac{1}{2\pi}\int_0^{2\pi} i_d(t)\left[V_o + R_{on} i_d(t)\right]dt = V_o I_{d,av} + R_{on} I_{d,rms}^2 \qquad (10)$$

Where $i_d(t)$, R_{on}, and V_o are the device current, on-state resistance, and the threshold voltage, respectively. Subscripts *av* and *rms* refer to average and RMS values, respectively. Equation (10) can be used to obtain the antiparallel diode conduction loss as well. Due to the pulsed current in auxiliary circuits of the TAC/Q2LC HB cells, and in CTB chain-links, the average and RMS auxiliary current values over the fundamental cycle are trivial, and the overall converter conduction losses will be dominated by the on-state losses in cells power path switches, bi state arms, or director valves. Also, it can be observed that in a F2F dc-dc converter, current flow in antiparallel diodes of the power feeding bridge (i.e. primary side converter in Fig. 3) takes place mainly during the voltage transition interval, leading to negligible average and RMS diode currents; hence, negligible antiparallel diode conduction loss in cells power path switches, bi state arms, or director valves. The above assumptions can be used to compare semiconductor losses among the three considered converter types.

The average and RMS values of arm/director valve current can be developed using (8) at $\gamma_r = 1$. The approximate conduction loss in the primary side can thus be developed using (8) and (10) as in (11) for the primary side converter being CTB, TAC, or Q2LC. If the primary converter is the power sending converter, V_o and R_{on} in (11) are of the employed IGBT devices. Otherwise, V_o and R_{on} in (11) are those of anti-parallel diodes.

$$P_{loss} = \frac{2NV_{dcp}\varphi}{3\omega_s L_s}\left(2V_o + R_{on}\frac{V_{dcp}\varphi}{\omega_s L_s}\right) \qquad (11)$$

Equation (11) will be used to clarify the relative conduction losses among the three converters of Fig. 1 using the implementation of Table I. When the same IGBT devices are used in the three converter types, the conduction losses expressed by (11) are equal for said three converter types at the same operating conditions. In section VI, (11) will be updated to reflect the relative conduction losses when low loss devices are utilized in bi-state arms of the TAC and in director valves of the CTB.

Table III concludes the characteristics of each type of converter, as discussed along section IV, normalized to the Q2LC case. It shows that the Q2LC merits a fully modular design while the TAC requires lowest silicon area and energy storage among the three candidates. However, modularity of TAC can be recovered as will be shown in section V. Furthermore, both TAC and CTB offer the possibility of use of thyristors as pointed out earlier, thus improving overall converter efficiency.

TABLE III
COMPARISON BETWEEN THE THREE CONVERTERS (PER UNIT VALUES NORMALIZED TO THE Q2LC)

	CTB	TAC	Q2LC
Nº of levels	*N*+1	*N*+1	*N*+1
Semicon. effort (pu)	1	7/8	1
Nº of capacitors (pu)	0.5	0.5	1
Capacitor voltage (pu)	0.5	1	1
Cell capacitance (pu)	2	0.5	1
Energy storage (pu)	0.25	0.25	1
Conduction loss (pu)	1	1	1
Use of Low loss semiconductors	Possible	Possible	Not possible

V. MODULAR TAC STRUCTURE

Although section II-A has shown that the bi-state arms of TAC switch on and off at near zero volt (zero ideally) regardless of loading conditions, simple RCD snubbers are still required to ensure uniform voltage sharing under transient conditions. However, when TAC is modularized such that the voltage of each semiconductor switch in the bi-state arm is effectively clamped by a cell capacitor, voltage sharing circuitry may not be required. Beside the merits of a modular design in terms of manufacturing economics, scalability, and reliability, such modular TAC design may also facilitate the use of low-loss force commutated devices such as the IGCT. Series connection of IGCTs has proven to require complex design even at medium voltage levels (e.g. medium voltage drives); that is why a modular design in which each IGCT is clamped by a cell voltage and switched under zero volt may be viable for TAC designs operating at suitable frequency ranges (< 1kHz). It is proposed here that IGCTs be used only in bi-state arms, not HB cells due to the fine switching sequence required to achieve the brief voltage transitions.

A. Modular Transition Arm Converter (MTAC)

The MTAC is obtained by reconfiguring the TAC such that the transition arm is split along the phase leg. Thus, each arm of the MTAC comprises a transition member (½*N* HB cells) and a director valve (½*N* switches) as in Fig. 5a. Full modularity can be achieved by augmenting each switch of the director valve into a HB cell of the transition member as in Fig. 5b. This way the voltage across the switch can be clamped when a clamp diode is connected as in Fig. 5b. The switching states of each cell given in Fig. 6 indicate that the clamp diode is continually reverse biased with no forward current flow in all cell states; hence, low current diode is sufficient. To clamp the off-state voltage of switch *S* to cell capacitor voltage, the clamp diode must exhibit controlled avalanche characteristics where the avalanche voltage (reverse blocking voltage) is double the nominal cell voltage. It is worth noting that the modular and hybrid MTAC designs are functionally equivalent. Also, in Figs. 5 and 6, the director switch *S* in each cell of the modular MTAC is depicted as an IGBT/diode pair although it can also be an IGCT/diode pair.

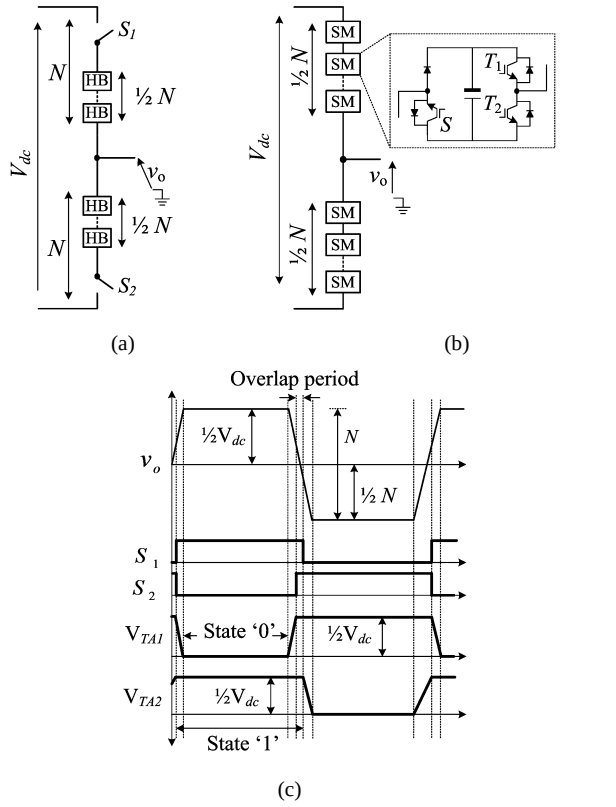


Fig.5 Symmetric TAC (STAC) configurations (a) Hybrid STAC structure, (b) Modular STAC structure, and (c) Schematic of the switching sequence of a generic STAC [subscripts *TA1* and *TA2* refer to the upper transition member and lower transition member, respectively].

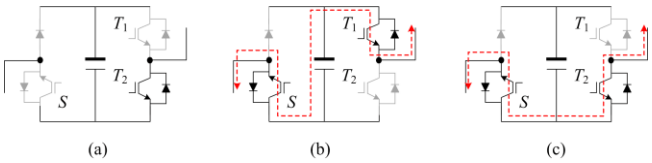


Fig. 6 Switching states of the modular STAC cell: (a) the idle state where no current flow possible, (b) the +V state where cell capacitor is inserted in conduction path, and (c) the 0V state in which cell capacitor is bypassed. [Grey traces denote the semiconductor device is in blocking state – Red traces represent current flow paths]

Unlike TAC, each arm of a MTAC phase leg synthesizes a half of the ac pole trapezoidal voltage. In doing so, the MTAC can be easily controlled under appropriate switching sequences to ensure near-zero net energy exchange for each phase leg over the fundamental cycle. One possible switching sequence is depicted graphically in Fig. 5c. When the ac pole of an MTAC phase leg is tied to the positive dc rail, upper arm director switch S_1 is on and upper arm HB cells are in state '0', while lower arm director switch S_2 is off and lower arm HB cells are in state '1'. Similarly, when the ac pole is tied to the negative dc rail, lower arm director switch S_2 is on and lower arm HB cells are in state '0', while upper arm director switch S_1 is off and upper arm HB cells are in state '1'. AC pole voltage transition from positive to negative dc rail is administered as follows:

- Upper arm HB cells switch sequentially to state '1' with inter time step T_d.
- Director switch S_2 is turned on and balancing common-mode current flows in the phase leg to balance its aggregate voltage with the dc link.
- Director switch S_1 is turned off; then lower arm HB cells switch sequentially to state '0' with inter time step T_d to tie the ac pole to negative dc rail.

AC pole voltage transition from negative to positive dc rail follows the same switching concept. The time interval during which both upper and lower router switches S_1 and S_2 are on and all HB cells in the phase leg are in state '1' is denoted an 'overlap interval'. This overlap is mandatory to ensure the net energy exchange of each hybrid arm over a fundamental cycle is near zero. Observe that operation of the MTAC as part of a F2F dc-dc converter with high gradient trapezoidal ac waveforms means that arm currents are also given by (1). Cell capacitors in each arm carry full load current for only half the voltage transition cycle T_t. It follows from the derivation of (7) that the MTAC requires nearly half the HB cell capacitance designed for an equivalent TAC. Therefore, energy excursions of MTAC arms are likewise limited and common-mode currents during the overlap interval are not significant.

To validate the MTAC design, the same simulation set-up of section III is repeated with the modular MTAC employed in replacement of the TAC in the F2F converter. For expedience, director switches and HB cells employ the same IGBT devices as in section III. Here T_d = 10µs. The two arm currents and cells voltages of one phase leg are depicted in Fig. 7. It can be observed that the capacitor voltages balance with the dc link during the 10µs-overlap interval, which is repeated each half fundamental cycle in the simulation set up (although overlap is shown once per cycle in Fig. 5c). The balance is achieved by the conventional sorting algorithm as in the TAC. Fig. 7 depicts also the voltage across the director switches and clamp diodes of one arm. It can be seen that the director switch voltages never exceed cell voltages. They sum up to the dc link voltage minus the sum of the cell voltages of the same arm. As expected, the clamp diodes do not conduct any forward current and they require near double the cell voltage rating.

B. Shunt Transition Arm Converter (STAC)

The conduction loss of each MTAC submodule can be further reduced by connecting an IGCT *S'* in parallel to the IGBT/diode pair T_2 as shown in Fig. 8a. This way, the STAC would feature improved efficiency relative to TAC and the MTAC since the phase current flows in low-loss devices for most of the fundamental cycle. Referring to STAC equivalent hybrid structure in Fig. 8b, the power and auxiliary switches T_1 and T_2 are both in the auxiliary path conducting load current only during voltage transit. Hence, both switches are of partial current rating. With reference to Table II, simple calculations show that the overall semiconductor effort of STAC is $9NV_dI_d$, which is roughly 12% higher than that of a Q2LC or a CTB.

On the other hand, the relative curtailment of conduction losses offered by STAC can be quantified for the current case study by updating (11) as in (12), where A and B are given in Table IV for different converter structures. In Table IV, superscripts refer to device type.

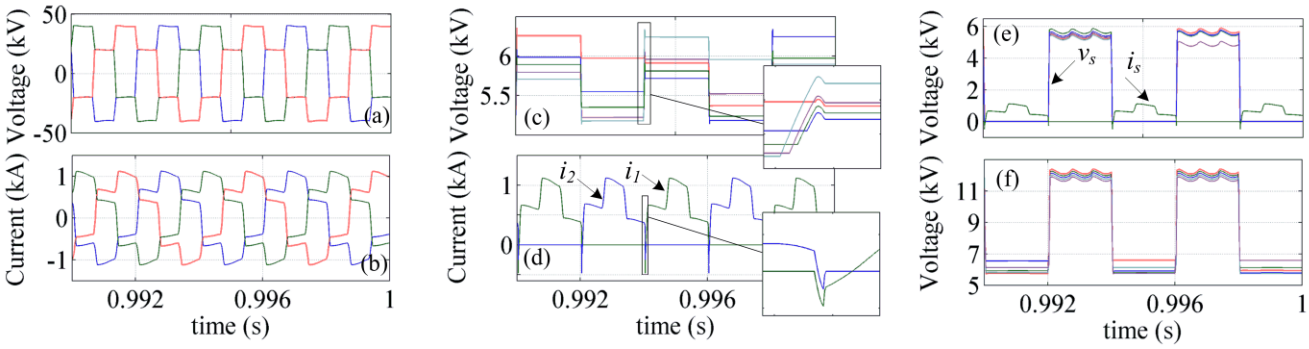


Fig. 7 Numerical simulation results of the modular TAC (MTAC) with the same F2F converter simulation setup of section III: (a) primary-side three-phase ac pole-to-neutral voltages, (b) primary-side three-phase ac pole currents, (c) cell voltages of the lower arm of one phase leg, (d) arm currents of said phase leg [i_1: upper arm current, i_2: lower arm current], (e) the voltages (v_s) and current (i_s) of director switches in the lower arm of said phase leg, and (f) Reverse voltages across clamp diodes in the same arm of (e).

$$P_{loss} = \frac{2NV_{dcp}\varphi}{3\omega_s L_s}\left(\mathrm{A} + \mathrm{B}\frac{V_{dcp}\varphi}{\omega_s L_s}\right) \tag{12}$$

TABLE IV
PARAMETERS A AND B OF EQUATION (11) FOR DIFFERENT CONVERTERS

	CTB, TAC, Q2LC	MTAC	STAC
A	$2V_o^{IGBT}$	$V_o^{IGBT} + V_o^{IGCT}$	$2V_o^{IGCT}$
B	R_{on}^{IGBT}	$\frac{1}{2}(R_{on}^{IGBT} + R_{on}^{IGCT})$	R_{on}^{IGCT}

Applying (12) to the MTAC and STAC in the F2F converter set up of section III – assuming each switch S or S' is the ABB 5SHY 35L4520 IGCTs are used – the conduction loss is about 85% (for the MTAC) and 75% (for the STAC) of that of the TAC, Q2LC, or the CTB at same operating conditions. Clearly exact conduction loss is subject to utilized semiconductor devices. However, it can be concluded from above figures that the STAC is more efficient that an equivalent MTAC. It can be seen also that both MTAC and STAC have an efficiency advantage over TAC and the Q2LC should they employ low-loss devices as appropriate.

In STAC, when the ac pole voltage is at one of the two dominant voltage levels ($\pm$½V_{dc}), the switch S' can be switched on to conduct ac pole current and the IGBT of T_2 remains off. When the S2TAC becomes the power-receiving converter in a bidirectional F2F dc-dc converter, ac pole current will flow dominantly through the freewheeling diode of T_2. Thus, this diode should be of low conduction loss with respect to the IGBT T_2. For that the IGBT and freewheeling diode may be discrete dyes. In the switching sequence shown in Fig. 8c, switches S and S' both turn on and off under zero voltage.

The STAC switching sequence of Fig. 8c is very similar to MTAC switching sequence of Fig. 5c except that shortly after the ac pole voltage is at either of the dominant voltage levels (+½V_{dc} or –½V_{dc}), the respective transition member submodules are switched simultaneously to idle state, idle state being shown in Fig. 9c. Only briefly before the next ac voltage transition, the submodules in the arm conducting load current switch simultaneously to state ‘0’ (Fig. 9b), then switch

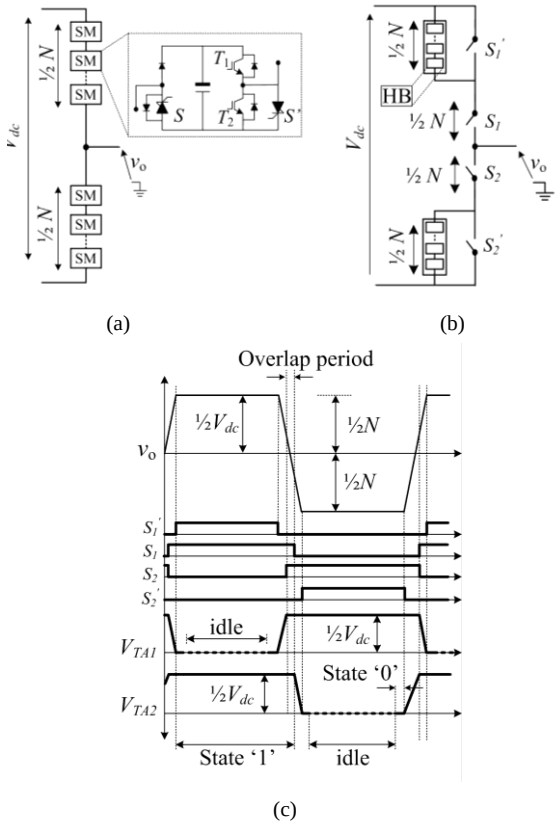


Fig. 8 Modular shunt TAC (MSTAC) configurations (a) Modular structure, (b), hybrid structure, and (c) Schematic of the switching sequence of a generic MSTAC [subscripts *TA1* and *TA2* refer to the upper transition member and lower transition member, respectively].

sequentially to state ‘1’ (Fig. 9d) once the shunt director switches S' turn off. The submodule ‘off’ state depicted in Fig. 9a is used when the relevant arm is in off state and the ac pole current flows in the complementary arm of the same phase leg. It can be observed from Fig. 9 that in all utilized switching states, the switch S' voltage is clamped by the cell capacitor. Also, the clamp diode is reverse biased and conducts no forward current.

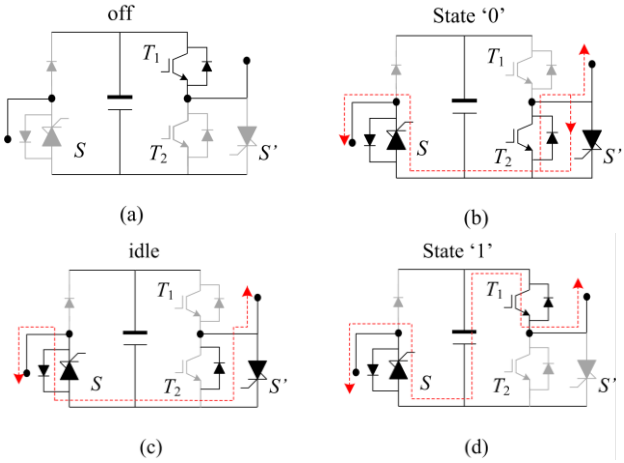


Fig. 9 Switching states of the modular shunt TAC submodule: (a) the off state where no current flow possible, (b) the 0V state where cell capacitor is inserted in conduction path, and (c) the 0V state in which cell capacitor is bypassed. [Grey traces denote the semiconductor device is in blocking state – Red traces represent current flow paths]

Fig. 10 depicts numerical simulation results of the STAC as part of the F2F dc-dc converter simulation set up of section III, where the STAC is the power-sending primary side converter. It is evident from Figs. 10c, 10d, and 10h that the switches T_2 and T_1 experience only pulsed current flow, confirming said low current rating requirement. The ac pole current can be seen to flow dominantly through switches S and S' whose voltages are clamped to the submodule voltage.

It is worth noting that when IGCT devices are used in the MTAC and STAC designs, associated di/dt reactor snubbers must be utilized to limit rate of current rise upon IGCT turn on. In this case, the overlap interval may need to be extended to allow natural current commutation between arms without voltage spikes. This aspect requires more in depth study.

VI. TAC Experimental Proof of Concept

Due to space limits and the fact that TAC, MTAC, and STAC are functionally equivalent, this section will provide experimental validation of TAC concept using a 1-kW scaled test rig. The primary purposes herein are:

- To confirm that proper trapezoidal operation of dc/ac TAC is possible with low energy storage in transition arms.
- To validate the sufficiency of a sorting algorithm for cell voltage balancing in transition arms without a further control action.
- To validate that triggered common-mode balancing currents are low and require no/minimal dedicated arm inductances.
- To confirm the pulsed current flow in auxiliary circuits of HB cells under trapezoidal operation of TAC.
- To reconfirm the insignificant current flow (hence low on-state loss) in antiparallel diodes in bi-state and transition arms.

It is sufficient for the experimental proof of the above properties to utilize the single-phase-leg dc/ac transition arm converter of Fig. 11 to synthesize trapezoidal ac waveform across the terminals of a lightly inductive passive load. TAC operation herein with a lightly inductive load resembles the operation of TAC in F2F dc-dc converters for dc grid applications where low-load-angle operation is typical [17]. In Fig. 11, said single phase single-leg TAC comprises an upper

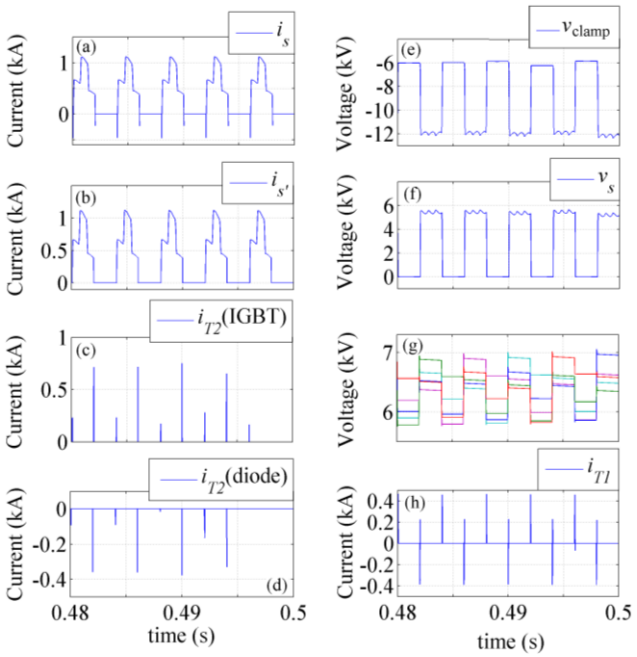


Fig. 10 Numerical simulation results of the modular shunt TAC (STAC) with the same F2F converter simulation setup of section III: (a) upper arm current of one phase leg (which is also switch S current), (b) Current in the shunt switch S', (c)Current in the IGBT T_2 of one submodule, (d) switch T_2 anti-parallel diode current in said submodule, (e) voltage across the clamp diode of said submodule (f) voltage across switch S of said submodule, (g) submodule voltages in said upper arm, and (h) current in the auxiliary switch T_1 of said submodule.

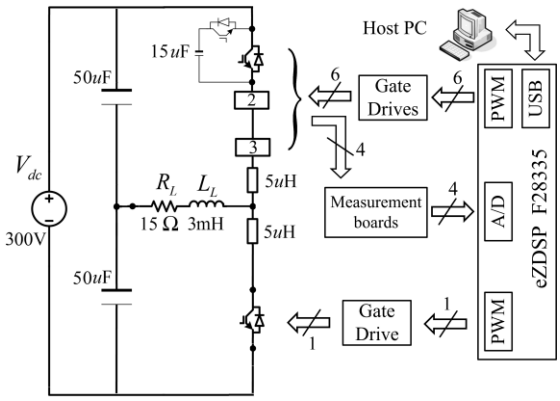


Fig.11 Schematic of the 1-kW single phase scaled TAC test rig.

transition arm and a lower bi-state arm. The transition arm comprises three HB cells and, thus, TAC is controlled to generate a 4-level trapezoidal ac voltage output across a passive load. The TAC is supplied from a 300V dc supply and a 50μF split capacitor provides a midpoint acting as a virtual ground reference point for the passive load to connect to. Consequently, peak load voltage is ±150V. IRG4IBC30UDPBF 17A 600V IGBTs are employed throughout. With 600V voltage rating, only one IGBT is connected in the bi-state arm to achieve the two-state operation therein. All other parameters are depicted in Fig. 11.

Gating signals generated by eZDSP F28335 control TAC operation such that said trapezoidal waveform is generated at

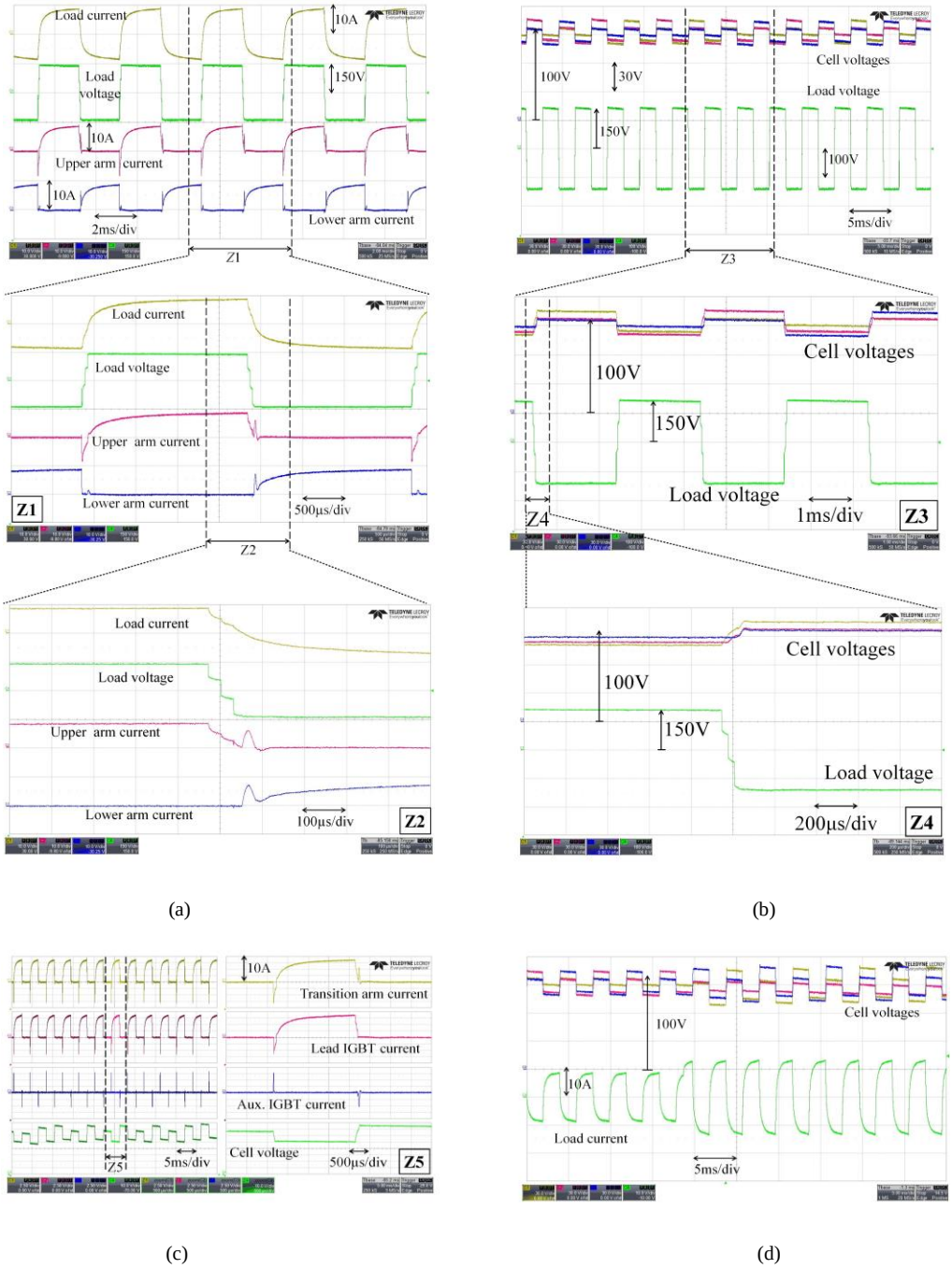


Fig.12 Proof of concept experimental results of the 1-kW single-phase TAC feeding a load.

a fundamental frequency of 250 Hz and a 30-µs dwell time in each intermediary voltage level between the two dominant voltage levels (i.e. T_t = 60µs). A 15µF capacitor is used in each HB cell and it is evident from Fig. 12b that this is sufficient to limit the cell voltage ripple to about ±15% around the nominal cell voltage of 100V, for about 18A peak-to-peak load current. This cell capacitance figure is significantly lower than that of an equivalent MMC of same dc voltage and loading conditions generating a sinusoidal voltage waveform across the load.

Fig. 12b shows further that transition arm cell voltages balance with proper action of the conventional sorting algorithm which can be seen clearly in the zoomed sections Z3 and Z4. It can be seen in zoomed section Z2 of Fig. 12a that the bi-state arm turns off following the voltage transition interval; expectedly triggering the depicted common-mode arm current pulse acting to balance transition arm voltage with the dc side. Here, the small 5µH arm inductance and the combined IGBT on-state resistance are sufficient to limit current slew rates and avoid any oscillations. The ac-side current is seen to be decoupled from such internal arm current dynamics. It can be deduced from zoomed section Z2 of Fig. 12a that the instant of bi-state arm switching (the instant the common-mode current

is triggered) corresponds to an ac pole voltage of –150V. This confirms the zero voltage switching property of the bi-state arm.

Further results collected from the test rig shows that all TAC auxiliary path circuits endure current pulses of about 8A peak twice per cycle (Fig. 12c). This is further illustrated in section Z5 of Fig. 12c for one cell of the transition arm. This is in line with the discussion in section III. Such intermittent current pattern reconfirms the low semiconductor ratings required for TAC auxiliary circuits relative to power path and bi-state arm semiconductor switches. Notice in Fig. 12c the brief current flow in the reverse direction in the bi-state arm as well as in the transition arm, which confirms the insignificance of anti-parallel diode on-state losses, as proposed in section IV.E. This is particularly true under high power factor loading, which is typical for the considered dc-dc conversion application (low loading angles) as has been shown in section III.

In Fig. 12d load current and cell voltages are depicted for a sudden 30% step load current rise. It is observed in Fig. 12d that transition arm capacitors remain seamlessly balanced after the step loading rise. The underlying reason is that the small energy capacity of the transition arm leads to nearly instant increase of cell voltage ripple band without energy oscillations. Also, comparing the experimented TAC to a Q2LC at the same dc voltage and loading, as experimented in [17], the latter exhibited some 40% higher cell voltage ripple for the same cell capacitance value. This reconfirms that TAC requires relatively lower cell capacitance; which was expected by the analysis of section IV-B.

VII. Conclusion

With emphasis on dc-dc conversion applications, this paper proposed a class of hybrid and modular multilevel converters denoted ‘transition arm converters’ (TAC) suited for operation with trapezoidal ac voltage waveforms. When employed in front-to-front medium and high voltage dc-dc converters of medium transformation ratios, the considered TAC converters provide further advantages over counterparts, specifically the quasi two level converter (Q2LC) proposed in [16]. It was shown that TAC converter requires about 12% less power electronics and quarter the energy storage required in an equivalent Q2LC. The loss of modularity in TAC has been remedied by proposing two modular TAC structures in which bi-state arms were modularized into transition arm cells. The resulting structures have been shown to provisionally facilitate the use of forced commutated semiconductors such as the IGCT to improve converter efficiency. Further investigations are still required though. The paper also touched upon the possible use of thyristors in director switches and bi-state arms for enhanced efficiency. The merits offered by TAC structures contribute to a better design compromise of isolated HVdc-dc converter in terms of cost, efficiency, and power density.

Coupling transformers tolerating non-sinusoidal excitation at efficiency standards comparable to these of conventional ac power transformers are required for the considered isolated dc-dc converters. As shown in [18], the resulting hysteresis curve of a six-step waveform excitation fortunately confines less area than that of corresponding sinusoidal excitation, promising slightly lower iron losses. Testing at no load using an Epstein frame confirmed slightly lower core losses than for the corresponding sinusoidal excitation [18]. Generally, trading off power density and losses is essential on designing the coupling transformer; particularly since, beyond a certain limit, the increase in power density is likely to be limited by creepage and clearance requirements of high voltage designs.

Overall, in the absence of efficient transformerless medium/high voltage dc-dc conversion solutions, research towards efficient medium frequency transformers with non-sinusoidal excitation should actively be pursued. The six-step trapezoidal excitation advocated in this paper may constitute a step in this direction.

VIII. References

[1] C.D. Barker, D.R. Trainer, R.S. Whitehouse., "Requirements of DC-DC converters to facilitate large DC grids" *SC B4 HVDC and Power Electronics* 2012.

[2] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday and B. W. Williams, "Modular multilevel structure of a high power dual active bridge DC transformer with stepped two-level output," *2014 16th European Conference on Power Electronics and Applications*, Lappeenranta, 2014, pp. 1-10.

[3] D. S. Gautam and A. K. S. Bhat, "A Comparison of Soft-Switched DC-to-DC Converters for Electrolyzer Application," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 54-63, 2013.

[4] C. Honnyong, D. Rongjun, T. Qingsong, and F. Z. Peng, "Design and Development of High-Power DC–DC Converter for Metro Vehicle System," *Industry Applications, IEEE Transactions on*, vol. 44, pp. 1795-1804, 2008.

[5] T. Jimichi, H. Fujita, and H. Akagi, "A Dynamic Voltage Restorer Equipped With a High-Frequency Isolated DC–DC Converter," *Industry Applications, IEEE Transactions on*, vol. 47, pp. 169-175, 2011.

[6] D. Jovcic and B. T. Ooi, "Developing DC Transmission Networks Using DC Transformers," *Power Delivery, IEEE Transactions on*, vol. 25, pp. 2535-2543, 2010.

[7] A. K. Rathore, A. K. S. Bhat, and R. Oruganti, "Analysis, Design and Experimental Results of Wide Range ZVS Active-Clamped L-L Type Current-Fed DC/DC Converter for Fuel Cells to Utility Interface," *Industrial Electronics, IEEE Transactions on*, vol. 59, pp. 473-485, 2012.

[8] W. Zhan and L. Hui, "A Soft Switching Three-phase Current-fed Bidirectional DC-DC Converter With High Efficiency Over a Wide Input Voltage Range," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 669-684, 2012.

[9] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *Industry Applications, IEEE Transactions on*, vol. 27, pp. 63-73, 1991.

[10] B. Hua and C. Mi, "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge DC-DC Converters Using Novel Dual-Phase-Shift Control," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 2905-2914, 2008.

[11] G. G. Oggier, M. Ordonez, J. M. Galvez, and F. Luchino, "Fast Transient Boundary Control and Steady-State Operation of the Dual Active Bridge Converter Using the Natural Switching Surface," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 946-957, 2014.

[12] H. van Hoek, M. Neubert, and R. W. De Doncker, "Enhanced Modulation Strategy for a Three-Phase Dual Active Bridge Boosting Efficiency of an Electric Vehicle Converter," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 5499-5507, 2013.

[13] R. Withanage and N. Shammas, "Series Connection of Insulated Gate Bipolar Transistors (IGBTs)," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 2204-2212, 2012.

[14] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, *et al*., "The Alternate Arm Converter: A New Hybrid Multilevel Converter With DC-Fault Blocking Capability," *Power Delivery, IEEE Transactions on*, vol. 29, pp. 310-317, 2014.

[15] T. Luth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-Frequency Operation of a DC/AC/DC System for HVDC

Applications," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 4107-4115, 2014.

[16] I.A. Gowaid, G.P. Adam, A.M. Massoud, S. Ahmed, D. Holliday, and B.W. Williams, "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability," in *Power Electronics, IEEE Transactions on*, vol.30, no.1, pp.108-123, Jan. 2015

[17] I.A. Gowaid, G.P. Adam, S. Ahmed, D. Holliday, and B.W. Williams, "Analysis and Design of a Modular Multilevel Converter With Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers," in *Power Electronics, IEEE Transactions on*, vol.30, no.10, pp.5439-5457, Oct. 2015

[18] N. Soltau, D. Eggers, K. Hameyer, and R. W. De Doncker, "Iron Losses in a Medium-Frequency Transformer Operated in a High-Power DC-DC Converter," *Magnetics, IEEE Transactions on*, vol. 50, pp. 953-956, 2014.

[19] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, "Comparison of the Modular Multilevel DC Converter and the Dual-Active Bridge Converter for Power Conversion in HVDC and MVDC Grids," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 124-137, 2015.

[20] J. W. K. a. G. Ortiz, "Solid-State-Transformers: Key Components of Future Traction and Smart Grid Systems," *IEEE International Power Electronics Conference - ECCE Asia*, May 2014.

[21] S. Kenzelmann, D. Dujic, F. Canales, Y. R. De Novaes, and A. Rufer, "Modular DC/DC converter: Comparison of modulation methods," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, 2012, pp. LS2a.1-1-LS2a.1-7.

[22] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. De Novaes, "Isolated DC/DC Structure Based on Modular Multilevel Converter," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 89-98, 2015.

[23] J. Yang, Z. He, H. Pang, and G. Tang, "The Hybrid Cascaded DC-DC Converters Suitable for HVDC Applications," *Power Electronics, IEEE Transactions on*, vol. PP, pp. 1-1, 2015.

[24] M. Hajian, J. Robinson, D. Jovcic, and W. Bin, "30 kW, 200 V/900 V, Thyristor LCL DC/DC Converter Laboratory Prototype Design and Testing," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 1094-1102, 2014.

[25] G. J. Kish, M. Ranjram, and P. W. Lehn, "A Modular Multilevel DC/DC Converter With Fault Blocking Capability for HVDC Interconnects," *Power Electronics, IEEE Transactions on*, vol. 30, pp. 148-162, 2015.

[26] T. Luth, M. M. C. Merlin, and T. C. Green, "Modular multilevel DC/DC converter architectures for HVDC taps," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[27] A. Schon and M. M. Bakran, "A new HVDC-DC converter with inherent fault clearing capability," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1-10.

[28] J. A. Ferreira, "The Multilevel Modular DC Converter," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 4460-4465, 2013.

[29] I. A. Gowaid, G. P. Adam, B. W. Williams, A. M. Massoud, and S. Ahmed, "The transition arm multilevel converter -- A concept for medium and high voltage DC-DC transformers," in *Industrial Technology (ICIT), 2015 IEEE International Conference on*, 2015, pp. 3099-3104.

[30] C. Oates, K. Dyke, and D. Trainer, "The use of trapezoid waveforms within converters for HVDC," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[31] P. K. B. Jacobson, G. Asplund, L. Harnefors, T. Jonsson, "VSC-HVDC Transmission with Cascaded Two-Level Converters," *Cigre 2010, B4-110*, 2010.

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